In re Patent Application of:
GUINEA ET AL.
Serial No. **09/784,549**
Filing Date: **FEBRUARY 15, 2001**

In the Claims:

Claims 1-28 (Cancelled).

29. (Currently amended) A circuit for recovering data from a serial data flow comprising:

a generator for generating a plurality of clock signals of equal period that are delayed equally relative to one another by a fraction equal to the period divided by a number of the plurality of clock signals;

a switching circuit for receiving the plurality of clock signals and providing one of the clock signals as an output thereof;

a phase comparator for receiving the output from said switching circuit and a data flow signal comprising a flow of data and providing at least one phase difference signal indicating a phase difference therebetween; ~~and~~

a data sampler receiving as inputs the data flow signal and the output of said switching circuit, and synchronizing sampling of the data flow signal based upon the output of said switching circuit; and

a controller for receiving the at least one phase difference signal from said phase comparator and controlling the switching circuit based thereon to switch the output of said switching circuit to one of said clock signals providing a smaller phase difference than a current clock signal;

said switching circuit providing the output synchronously with a transition of the output and before disabling a current output to substantially prevent the production of false signals during switching.

30. (Previously presented) The circuit according to Claim 29 wherein said generator comprises a delay-locked loop circuit.

Claims 31-35 (cancelled).

36. (New) The circuit according to Claim 29 wherein said switching circuit comprises a plurality of circuits each receiving a respective one of the plurality of clock signals as an input thereto and selectively outputting the input as the output of said switching circuit.

37. (New) The circuit according to Claim 36 wherein said plurality of circuits are connected in a ring; and wherein each of said plurality of circuits provides a respective disabling signal upon being selected to adjacent circuits in the ring to disable said adjacent circuits.

38. (New) The circuit according to Claim 37 wherein said switching circuit further comprises a decoding circuit for receiving at least one control signal from said controller and providing at least one selection signal for activating one of

said plurality of circuits based upon on a state of the at least one control signal.

39. (New) The circuit according to Claim 38 wherein each of the clock signals is delayed equally relative to one another by a fraction equal to the period divided by a number of said plurality of circuits.

40. (New) The circuit according to Claim 38 wherein each disabling signal comprises a pulse; and wherein each of said plurality of circuits generates its respective pulse based upon the at least one selection signal.

41. (New) The circuit according to Claim 40 wherein each of said plurality of circuits provides an enabling signal for enabling the transmission of its respective clock signal based upon the at least one selection signal, the enabling signal being activated synchronously with a trailing edge of the respective clock signal.

42. (New) The circuit according to Claim 41 wherein each of said plurality of circuits deactivates its respective enabling signal upon receiving the disabling signal.

43. (New) A method for recovering data from a serial data flow comprising:

generating a plurality of clock signals of equal period

that are delayed equally relative to one another by a fraction equal to the period divided by a number of the plurality of clock signals;

receiving the plurality of clock signals at a switching circuit and providing one of the clock signals as an output thereof;

providing at least one phase difference signal indicating a phase difference between the output from the switching circuit and a data flow signal comprising a flow of data;

synchronizing sampling of the data flow signal based upon the output of the switching circuit; and

controlling the switching circuit based upon the at least one phase difference signal to switch the output of the switching circuit to one of the clock signals providing a smaller phase difference than a current clock signal and so that the switching circuit provides the output synchronously with a transition of the output and before disabling a current output to substantially prevent the production of false signals during switching.

44. (New) The method according to Claim 43 wherein generating comprises generating the plurality of clock signals using a delay-locked loop circuit.

45. (New) The method according to Claim 43 wherein the switching circuit comprises a plurality of circuits each

receiving a respective one of the plurality of clock signals as an input thereto and selectively outputting the input as the output of the switching circuit.

46. (New) The method according to Claim 45 wherein the plurality of circuits are connected in a ring; and wherein each of the plurality of circuits provides a respective disabling signal upon being selected to adjacent circuits in the ring to disable the adjacent circuits.

47. (New) The method according to Claim 46 wherein controlling comprises controlling using at least one control signals; and wherein the switching circuit further comprises a decoding circuit for receiving at least one control signal and providing at least one selection signal for activating one of the plurality of circuits based upon on a state of the at least one control signal.

48. (New) The method according to Claim 47 wherein each of the clock signals is delayed equally relative to one another by a fraction equal to the period divided by a number of the plurality of circuits.

49. (New) The method according to Claim 47 wherein each disabling signal comprises a pulse; and wherein each of the plurality of circuits generates its respective pulse based upon the at least one selection signal.

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50. (New) The method according to Claim 49 wherein each of the plurality of circuits provides an enabling signal for enabling the transmission of its respective clock signal based upon the at least one selection signal, the enabling signal being activated synchronously with a trailing edge of the respective clock signal.

51. (New) The method according to Claim 50 wherein each of the plurality of circuits deactivates its respective enabling signal upon receiving the disabling signal.